

1/3

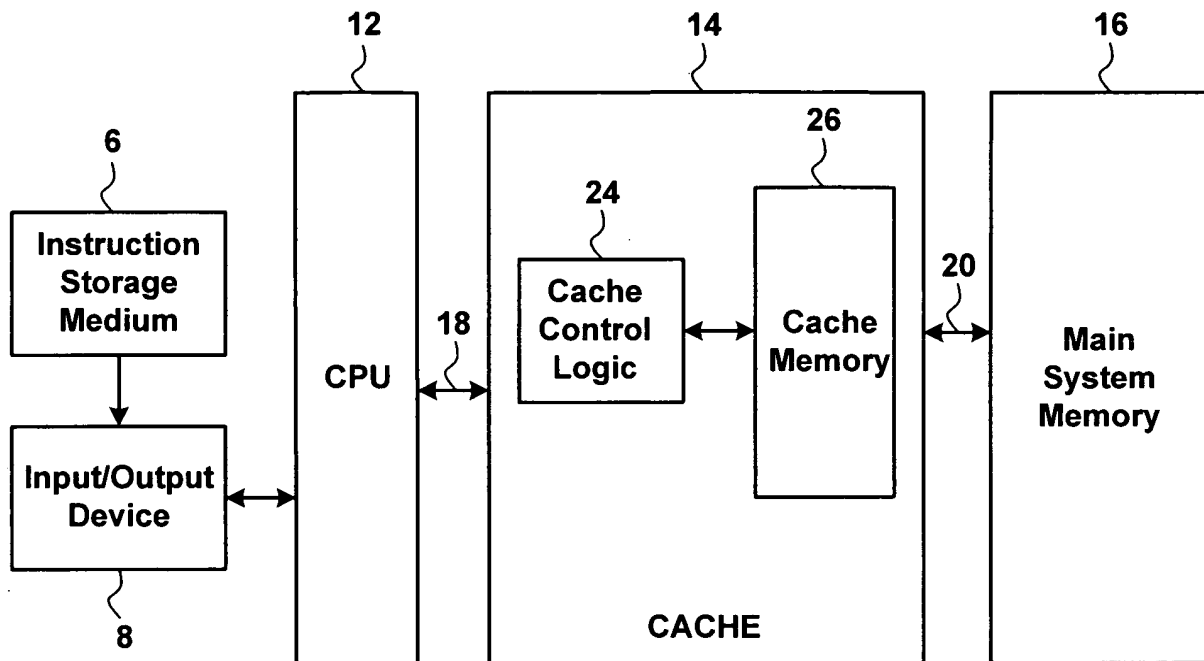


Figure 1

P	30	31	32	33	34	35	36	37	38	39	40	41
Q	Sequence	a	b	a	c	d	b	b	e	a	c	d
LRU=>	Allocation	a=>0	b=>1		c=>2	d=>3			e=>0	a=>2	c=>3	d=>1
R	0/w	1/x	2/y	2/y	3/z	1/b	0/a	0/a	2/c	3/d	1/b	0/e
S	1/x	2/y	3/z	3/z	1/b	0/a	2/c	2/c	3/d	1/b	0/e	2/a
T	2/y	3/z	0/a	1/b	0/a	2/c	3/d	3/d	1/b	0/e	2/a	3/c
U	3/z	0/a	1/b	0/a	2/c	3/d	1/b	1/b	0/e	2/a	3/c	1/d
V	Replaced	w==>	x==>		y==>	z==>			a==>	c==>	d==>	b==>

Figure 2
(Prior Art)

P	Q	R	S	T	U	V	Sequence	a	b	a	c	d	b	RICL (b)	e	a	c	d
LRU=>							Allocation	a==>0	b==>1		c==>2	d==>3			e==>1			
							0/w	1/x	2/y	2/y	3/z	1/b	0/a	1/b	0/a	2/c	3/d	1/e
							1/x	2/y	3/z	3/z	1/b	0/a	2/c	0/a	2/c	3/d	1/e	0/a
							2/y	3/z	0/a	1/b	0/a	2/c	3/d	2c	3/d	1/e	0/a	2/c
							3/z	0/a	1/b	0/a	2/c	3/d	1/b	3/d	1/e	0a	2/c	3/d
							Replaced	w==>	x==>		y==>	z==>			b==>			

Importance level
of cache line is
reduced; cache
line b continues
to store valid data

Figure 3